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Remarks

Applicant and his representatives wish to thank Examiner Wilson for the thorough examination of the present application and the detailed explanations in the Office Action dated December 16, 2005.

Claims 3-4 have been cancelled. New Claim 21 has been added. Thus, claims 1-2 and 5-21 are active in the present application. No new matter is introduced by the present Amendment.

The present invention relates to a method for fabricating a metal / insulator / metal capacitor comprising a first metal layer, a dielectric layer, and a second metal layer. The claimed method comprises etching the second metal layer, and etching the dielectric layer under conditions different from etching the second metal layer, to leave a residual dielectric layer over the first metal layer in an etched part of the dielectric layer (see claim 1 as amended above). By leaving a residual dielectric layer over the first metal layer in an etched part of the dielectric layer, the method may result in improved metal / insulator / metal characteristics, increased stability of the metal etching process, and increased margin for subsequent processes (see, e.g., paragraph [0026] of the present specification).

The references cited against the originally filed claims neither disclose nor suggest, alone or taken together, a method for fabricating a metal / insulator / metal (MIM) capacitor comprising etching a dielectric layer (of the capacitor) under conditions different from etching the top metal layer, to leave a residual dielectric layer over the bottom metal layer in an etched part of the dielectric layer. Consequently, the claims, as amended, are believed to be patentable over the cited references.

The Rejection of Claims 1-4 and 19 under 35 U.S.C. § 102(b)

The rejection of Claims 1-4, 19 under 35 U.S.C. § 102(b) as being anticipated by Maejima et al. (US 6,891,218) is respectfully traversed.

Maejima et al. discloses a method of fabricating a capacitor with a first metal layer, a ferroelectric layer, and a second metal layer, wherein a photoresist layer is formed on the top metal layer and used as a mask to sequentially etch the metal layer and the ferroelectric layer. However, Maejima et al. does not disclose an etching step that leaves a residual dielectric layer over the bottom metal layer in an etched part of the dielectric layer.

Maejima et al. teaches a method where, as a result of etching the ferroelectric layer, the resulting etched ferroelectric layer has the same size of the photoresist layer (column 11, lines 13-14; FIG. 3F). Maejima et al. illustrates the process of etching the ferroelectric layer by showing an unetched ferroelectric layer 3 (see col. 10, ll. 36-43 and 54-55, and FIG. 3D), a partially etched ferroelectric layer 3 during the etching process (see col. 10, l. 56-col. 11, l. 12, and FIG. 3E), then a fully etched ferroelectric layer (column 11, lines 13-14, and FIG. 3F). Maejima et al. neither discloses nor suggests leaving a residual ferroelectric layer as a result of the etching step performed thereon.

In the present claims, a residual dielectric layer is left in the etched region thereof (see also paragraphs [0024]-[0026] and [0029] and FIG. 2 of the present application). Maejima et al. does not disclose a method of etching a dielectric layer in a method of making a MIM capacitor to leave a residual dielectric layer over a bottom metal layer in an etched part of the dielectric layer. Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejections of Claims 5 and 12 – 18 under 35 U.S.C. § 103(a)

The rejections of Claims 5 and 12 – 18 under 35 U.S.C. § 103 as being unpatentable over Maejima et al. in view of Hwang (US 2003/0064590) is respectfully traversed.

As discussed above, Maejima et al. is deficient with regard to etching a dielectric layer in a method of making a MIM capacitor to leave a residual dielectric layer over a bottom metal layer in an etched part of the dielectric layer. Hwang fails to cure this deficiency.

Hwang provides specific etchant gas formulations and parameters for optimally etching a Pt layer and a protective layer comprising Ti or TiN in high density integrated circuit semiconductor devices. The protective layer protects the corners of the etched Pt layer and provides good mask adhesion to the Pt layer for subsequent processes. However, since Hwang's etching gases and parameters relate to sequential etching of Pt and Ti or TiN layers, as opposed to etching a dielectric layer, it would not be obvious to one of ordinary skill in the art to use the etching parameters of Hwang in the method of Maejima et al. to etch a dielectric layer in a method of making a MIM capacitor to leave a residual dielectric layer over a bottom metal layer in an etched part of the dielectric layer.

Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejections of Claims 6 and 7 under 35 U.S.C. § 103(a)

The rejections of Claims 6 and 7 under 35 U.S.C. § 103 as being unpatentable over Maejima et al. in view of Ouellet et al. (US 6,083,805) is respectfully traversed.

As discussed above, Maejima et al. is deficient with regard to etching a dielectric layer in a method of making a MIM capacitor to leave a residual dielectric layer over a metal layer in an etched part of the dielectric layer. Ouellet et al. fails to cure this deficiency.

Ouellet et al. discloses a method of forming capacitors in a semiconductor device, involving providing a first insulating layer, providing a first mask with an array of apertures over the insulating layer, and etching an array of holes in the first insulating layer through said apertures in said first mask (Abstract). A first electrode layer extending into the holes is formed over the first insulating layer, a second dielectric layer extends into the holes on said first electrode layer, then a second electrode layer extends into the holes on the dielectric layer. The capacitors are then patterned with a second mask (Abstract). In one embodiment, a high value capacitor may be formed in a semiconductor device where a metal layer comprises a Ti/TiN composite layer.

However, Ouellet et al. appears to be silent with regard to etching a dielectric layer to leave a residual dielectric layer over a metal layer in an etched part of the dielectric layer. As a result, Ouellet et al. cannot cure the deficiency of Maejima et al. with regard to the present claims, and it would not be obvious to one of ordinary skill in the art to combine any part of the process disclosed by Ouellet et al. with the method of Maejima et al. to etch a dielectric layer in a method of making a MIM capacitor to leave a residual dielectric layer over a metal layer in an etched part of the dielectric layer.

Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejections of Claims 8 – 10 under 35 U.S.C. § 103(a)

The rejections of Claims 8 – 10 under 35 U.S.C. § 103 as being unpatentable over Maejima et al. in view of Allman et al. (US 2003/0068858) is respectfully traversed.

As discussed above, Maejima et al. is deficient with regard to etching a dielectric layer to leave a residual dielectric layer over a bottom metal layer in an etched part of the dielectric layer. Allman et al. fails to cure all of the deficiencies of Maejima et al.

Allman et al. teaches a method of forming a capacitor in a semiconductor device by etching an interconnect layer 24 that may include Ti, TiN, and Al layers (see paragraph [0022]), then embedding preferably the capacitor 20 within the space normally occupied by the vertical height dimension of the interconnect layer 24 (see paragraph [0024] and FIG. 1). To embed the capacitor 20 within the interconnect layer 24, substantially all of the layers 38 (e.g., Al) and 40 (e.g., TiN; see paragraph [0036]) of the interconnect layer 24 must be removed to form a cavity 45 to make a space to be occupied by the capacitor 20 (see paragraph [0024]). A dielectric material 42 is deposited on the lower titanium layer 36, and a layer of titanium nitride 44 deposited on top of the capacitor dielectric material 42 (see paragraph [0025]).

As shown in FIG. 7 of Allman et al., the top titanium nitride layer 51 is etched outside of the region covered by the photoresist 52 (see FIG. 6) by a conventional plasma process that

etches the material with directionality that is substantially vertical to the horizontal surfaces of the resist layer 52 (see paragraph [0035]). In this manner, outer edges of the top capacitor plate 44 remain substantially vertical. However, titanium nitride metal sidewall spacers 54 remain from the layer 51. These spacers 54 form no part of the capacitor 20 (FIG. 1) or interconnect layer 24, but do provide a smoother transition of the IMD layer 26 into the capacitor cavity, improving the final degree of subsequent planarity (see paragraph [0035] of Allman et al.). The dielectric layer 42 may be etched away along with and in the same region as the titanium nitride layer 51. An alternative, as illustrated by FIG. 1 of Allman et al., does not etch the dielectric layer 42 but instead leaves it in place to reduce electrical leakage of the capacitor 20. At the point in the process flow shown in FIG. 7, the structure of the capacitor 20 is essentially completed (see paragraph [0035] of Allman et al.).

However, Allman et al. do not appear to disclose the conditions for etching either the top titanium nitride layer 51 or the dielectric layer 42. Thus, Allman et al. appear to be silent with regard to etching a dielectric layer of a metal/insulator/metal capacitor under conditions different from etching the overlying metal layer, to leave a residual dielectric layer over the underlying metal layer in an etched part of the dielectric layer. As a result, Allman et al. fail to cure all of the deficiencies of Maejima et al. with regard to the present claims.

Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claim 11 under 35 U.S.C. § 103(a)

The rejections of Claim 11 under 35 U.S.C. § 103 as being unpatentable over Maejima et al. in view of Tee et al. (US 2002/0052077) is respectfully traversed.

As discussed above, Maejima et al. is deficient with regard to etching a dielectric layer to leave a residual dielectric layer over a bottom metal layer in an etched part of the dielectric layer. Tee et al. fails to cure all of the deficiencies of Maejima et al.

Tee et al. teaches a DRAM structure wherein the interconnect bus lines comprise a Ti, TiN, and AlCu laminate. However, in a first embodiment, a portion of the epitaxial layer grown on a silicon substrate is doped N^+ over an insulating layer to form capacitor bottom electrodes (paragraph [0013] of Tee et al.). Thereafter, a thin gate oxide is formed on the epitaxial layer, and a polysilicon layer is deposited thereon, doped N^+ by ion implantation, and then patterned to form FET gate electrodes over the openings in the first insulating layer and also to form capacitor top electrodes for the capacitors over the capacitor bottom electrodes (paragraph [0013] of Tee et al.). Although the polysilicon layer 22 can include an upper metal silicide layer (paragraph [0026] of Tee et al.), Tee et al. appear to disclose only a silicon-insulator-polysilicon capacitor. As a result, it is not clear that one skilled in the art would look to Tee et al. for a teaching of etching a dielectric layer of a metal/insulator/metal capacitor under conditions different from etching the overlying metal layer, to leave a residual dielectric layer over the underlying metal layer in an etched part of the dielectric layer. As a result, Tee et al. fail to cure the deficiencies of Maejima et al. with regard to the present claims.

Therefore, this ground of rejection is unsustainable, and should be withdrawn.

The Rejection of Claim 20 under 35 U.S.C. § 103(a)

The rejection of Claim 20 under 35 U.S.C. § 103 as being unpatentable over Maejima et al. in view of Subramanian et al. (US 5,494,837) is respectfully traversed.

As discussed above, Maejima et al. is deficient with regard to etching a dielectric layer to leave a residual dielectric layer over a bottom metal layer in an etched part of the dielectric layer. Subramanian et al. fails to cure all of the deficiencies of Maejima et al.

Subramanian et al. disclose a method of forming a semiconductor-on-insulator (SOI) electronic device includes the steps of etching a semiconductor substrate to form a plurality of adjacent trenches therein and then forming electrically insulating layers on bottoms of the trenches (Abstract). Epitaxial lateral overgrowth (ELO) is then performed to grow respective

monocrystalline semiconducting regions in the trenches. These semiconducting regions are preferably grown from a sidewall of each trench onto a respective insulating layer and fill each trench. Monocrystalline active regions of the electronic device are then formed in the semiconducting regions and also in the substrate, adjacent the trench sidewalls (see the Abstract of Subramanian et al.). However, Subramanian et al. appear to be silent with regard to capacitors or any method of making capacitors.

As a result, it is not clear that one skilled in the art would look to Subramanian et al. for a teaching of etching a dielectric layer of a metal/insulator/metal capacitor under conditions different from etching the overlying metal layer, to leave a residual dielectric layer over the underlying metal layer in an etched part of the dielectric layer. As a result, Subramanian et al. fail to cure the deficiencies of Maejima et al. with regard to the present claims.

Therefore, this ground of rejection is unsustainable, and should be withdrawn.

Conclusions

In view of the above amendments and remarks, all bases for objection and rejection are believed to be overcome, and the application is believed to be in condition for allowance. Early notice to that effect is earnestly requested.

If it is deemed helpful or beneficial to the efficient prosecution of the present application, the Examiner is invited to contact Applicant's undersigned representative by telephone.

Respectfully submitted,

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